

Hall Ticket Number:

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Code No. : 13648 S O

**VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD***Accredited by NAAC with A++ Grade***B.E. (I.T.) III-Semester Supplementary Examinations, August-2022****Basic Electronics**

Time: 3 hours

Max. Marks: 60

*Note: Answer all questions from Part-A and any FIVE from Part-B***Part-A (10 × 2 = 20 Marks)**

Q. No.	Stem of the question	M	L	CO	PO
1.	Distinguish between forward bias and reverse bias of a diode.	2	1	1	1
2.	State the application of a diode that specifically operates in reverse break down region.	2	1	1	1
3.	List out the different modes of operation of a BJT.	2	1	2	1
4.	Distinguish between the three configurations of a BJT.	2	1	2	1
5.	Draw the circuit symbols of NMOS and PMOS transistors.	2	1	3	1
6.	Draw the circuit of a CMOS NOT gate.	2	1	3	1
7.	State the Barkhausen's criteria of oscillations.	2	1	4	1
8.	List the advantages of negative feedback.	2	1	4	1
9.	List the ideal characteristics of an operational amplifier.	2	2	5	1
10.	Draw the pin diagram of Op Amp, labeling all the pins.	2	2	5	1
<b>Part-B (5 × 8 = 40 Marks)</b>					
11. a)	Explain the V-I characteristics of a diode. Also give the diode current equation and explain the terms involved.	4	2	1	1
b)	Draw and explain the operation of a bridge rectifier circuit.	4	2	1	1
12. a)	List out the different biasing circuits of a BJT. Derive the expression of stability factor for a voltage divider bias circuit of BJT.	4	2	2	1
b)	Draw the h parameter equivalent circuit of a BJT in common emitter configuration and define the different h parameters involved.	4	2	2	1
13. a)	Implement two input NAND gate using CMOS transistors and explain its operation.	4	3	3	1
b)	Compare the various digital integrated circuit logic families.	4	2	3	1

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14. a)	Draw the circuit diagram of Hartley oscillator and derive the expression of its frequency of oscillation.	4	3	4	1
b)	Derive the expression for loop gain of a negative feedback amplifier.	4	3	4	1
15. a)	Explain the operation of a square wavegenerator using an Op Amp and derive an expression for its frequency.	4	3	5	1
b)	Derive an expression of output voltageof an integrator circuit constructed using an Op Amp.	4	3	5	1
16. a)	With neat circuit diagram explain the operation of a positive clamping circuit.	4	3	1	1
b)	Derive the relationship between the large signal current gain of a common base and common emitter transistor.	4	3	2	1
17.	Answer any <i>two</i> of the following:				
a)	Explain the physical structure of CMOS transistor.	4	2	3	1
b)	Draw and explain the operation of a RC phase shift oscillator.	4	2	4	1
c)	Draw the circuit diagram and derive the output of a log amplifier constructed using Op Amp.	4	3	5	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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